CLAIMS

What is claimed is:

1. A circuit for determining the propagation delay of an integrated circuit, comprising:

a first rank of logic memory elements, each logic memory element having a data input, a data output, and a clock input, the clock inputs being coupled together and configured to be driven by a clock signal;

a plurality of delay units coupled in series, each delay unit having an input and an output, the output of each delay unit configured to drive the data input of one of the logic memory elements; and

a logic inverter having an input configured to be driven by the clock signal, the inverter having an output configured to drive the input of the first delay unit of the plurality of delay units.

2. The circuit of claim 1, wherein each of the plurality of delay units exhibits the same amount of delay.

3. The circuit of claim 1, wherein each delay unit comprises a plurality of logic inverters coupled in series.

4. The circuit of claim 3, wherein each delay unit of the second plurality of delay units comprises a plurality of logic inverters coupled in series.

5. The circuit of claim 1, wherein each logic memory element of the first rank comprises a D flip-flop.

6. The circuit of claim 1, further comprising a second rank of logic memory elements, each logic memory element of the second rank having a data input, a data output, and a clock input, the clock inputs being coupled together and configured to be driven by the clock signal, the data input of each logic memory element of the second rank configured to be driven by the data output of one of the logic memory elements of the first rank.

7. The circuit of claim 6, wherein each logic memory element of the second rank comprises a D flip-flop.

8. The circuit of claim 1, further comprising a preliminary delay unit configured to delay the clock signal prior to driving the input of the logic inverter.

9. The circuit of claim 1, further comprising a preliminary delay unit configured to delay the output of the logic inverter prior to driving the input of the first delay unit of the plurality of delay units.

10. The circuit of claim 1, further comprising a plurality of AND gates, each AND gate being associated with one of the series of delay units, each AND gate having an output configured to drive the data input of the logic memory element of the first rank associated with the delay unit associated with the AND gate, each AND gate having a first input configured to be driven by the output of its associated delay unit and a second input configured to be driven by the output of the logic memory element of the first rank associated with the delay unit immediately preceding the delay unit associated with the AND gate, the second input of the AND gate associated with the first delay unit of the series of delay units being configured to be driven by a logic HIGH.

11. The circuit of claim 1, further comprising:

a multiplexer having data inputs, selector inputs, and a data output;

a second plurality of delay units coupled in series, each delay unit of the second plurality of delay units having an input and an output, the output of each delay unit of the second plurality of delay units configured to drive one of the inputs of the multiplexer; and

a microprocessor configured to read the data output of each of the logical memory elements and to select one of the data inputs of the multiplexer via the selector inputs for gating to the output of the multiplexer.

12. A circuit for determining the propagation delay of an integrated circuit, comprising:

means for logically inverting a clock signal, resulting in an inverted clock signal;

means for delaying the propagation of the inverted clock signal multiple times, resulting in a plurality of delayed inverted clock signals, with each delayed inverted clock signal being delayed a different amount; and

means for storing the logical state of each of the delayed inverted clock signals at each pulse of the clock signal, resulting in a stored logical state for each of the delayed inverted clock signals.

13. The circuit of claim 12, wherein the plurality of delayed inverted clock signals is delayed in a linear fashion.

14. The circuit of claim 12, wherein the inverting means comprises a logic inverter.

15. The circuit of claim 12, further comprising a preliminary delay unit configured to delay the clock signal prior to driving the inverting means.

16. The circuit of claim 12, further comprising a preliminary delay unit configured to delay the inverted clock signal prior to driving the delaying means.

17. The circuit of claim 12, wherein the delaying means comprises a plurality of delay units coupled in series.

18. The circuit of claim 17, wherein each delay unit comprises a plurality of logic inverters coupled in series.

19. The circuit of claim 12, wherein the storing means comprises a first rank of logic memory elements, each logic memory element of the first rank configured to be clocked by the clock signal.

20. The circuit of claim 19, wherein each logic memory element of the first rank comprises a D flip-flop.

21. The circuit of claim 19, wherein the storing means further comprises a second rank of logic memory elements configured to be clocked by the clock signal, the second rank of logic memory elements storing the state of the first rank of logic memory elements.

22. The circuit of claim 21, wherein each logic memory element of the second rank comprises a D flip-flop.

23. The circuit of claim 12, further comprising means for forcing the stored logical state of each of the delayed inverted clock signals to collectively display a single logical transition indicating the propagation delay of the integrated circuit.

24. The circuit of claim 12, further comprising means for tuning the speed of a critical signal based on the stored logical state for each of the delayed inverted clock signals.

25. The circuit of claim 24, wherein the tuning means comprises:

means for delaying the propagation of the critical signal multiple times, resulting in a plurality of delayed critical signals, with each delayed critical signal being delayed a different amount; and

means for selecting one of the delayed critical signals.

26. The circuit of claim 25, wherein the delaying means of the tuning means comprises a plurality of delay units coupled in series.

27. The circuit of claim 26, wherein each delay unit of the tuning means comprises a plurality of logic inverters coupled in series.

28. The circuit of claim 25, wherein the selecting means comprises:

a multiplexer configured to gate one of the delayed critical signals for output; and

a microprocessor configured to read the logical state of each of the delayed inverted clock signals and to select one of the delayed critical signals for output by way of the multiplexer.

29. A method for determining the propagation delay of an integrated circuit, comprising:

logically inverting a clock signal, resulting in an inverted clock signal;

delaying the propagation of the inverted clock signal multiple times, resulting in a plurality of delayed inverted clock signals, with each delayed inverted clock signal being delayed a different amount; and

storing the logical state of each of the delayed inverted clock signals at each pulse of the clock signal, resulting in a stored logical state for each of the delayed inverted clock signals.

30. The method of claim 29, wherein the plurality of delayed inverted clock signals is delayed in a linear fashion.

31. The method of claim 29, further comprising forcing the stored logical state of each of the delayed inverted clock signals to collectively display a single logical transition indicating the propagation delay of the integrated circuit.

32. The method of claim 29, further comprising tuning the speed of a critical signal based on the stored logical state for each of the delayed inverted clock signals.